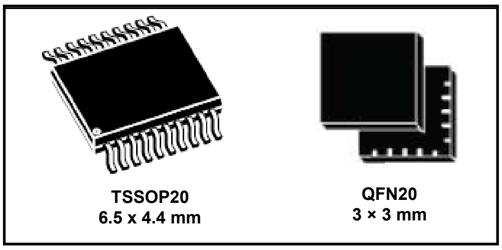
CX32L003
ARM® Cortex®-M0+ 32-bit Microcontroller
Datasheet

CX32L003

ARM® Cortex®-M0+ 32-bit MCU, up to 64 KB Flash, 4 KB SRAM, 2.5-5.5V, TSSOP-20/QFN-20

Datasheet - production data

- **Core**
  - ARM® Cortex®-M0+ core, up to 24 MHz
  - 24-bit system timer
  - Support Low-power sleep mode
  - Single-cycle 32-bit hardware multiplier
- **Memory**
  - 32K/64K Byte embedded Flash, with erase/write protection function
  - 4K Byte SRAM
- **Clock and power supply**
  - 4 optional clock sources
    - External 4 MHz~24 MHz high-frequency crystal oscillator
    - External 32.768 KHz crystal oscillator
    - Internal 4 MHz~24 MHz high-frequency clock
    - Internal 38.4 KHz/32.768 KHz low- frequency clock
    - Support hardware clock monitoring
  - Power management
    - Two low-power modes: Sleep Mode, Deep Sleep Mode
    - Low-voltage detection, which can be configured as interrupt or reset
- **Interrupt**
  - A nested vectored interrupt controller (NVIC) is used for controlling 32 interrupt sources, and 4 priorities can be set for each interrupt source.
  - Support serial wire debug (SWD), with 2 watch points/4 break points.
- **General I/O pins**
  - 16 I/Os on 20-pin package
- **Communication interface**
  - UART0-UART1 standard communication interface
  - Support ultra-low power UART with the low-frequency clock
  - SPI standard communication interface, up to 8 Mbps
  - I2C standard communication interface, up to 1 Mbps for master mode, and up to 800 Kbps for slave mode
  - One-Wire communication interface
- **Buzzer frequency generator**
  - It can generate a buzzing signal at 1 KHz, 2 KHz and 4 KHz



- **Timer/counter**
  - 1 × 16-bit advanced-control timer: 4 channels of PWM output/input capture; support 3-channel complementary output, dead time generation and emergency break input
  - 1 × 16-bit general-purpose timer: support 4-channel compare output/input capture, PWM output
  - 1 × 16-bit programmable counter array: support 5-channel input capture/compare output and PWM output
  - 2 × 16-bit/32-bit basic timer/counter
  - 1 × 16-bit low-power timer (LPTIM)
  - Automatic wake-up timer
  - System window watchdog (WWDG) and independent watchdog timer (IWDG)
- **RTC**
  - Support RTC counting (second/minute/hour) and calendar function (dd/mm/yy)
  - Support RTC alarm function register (second/minute/hour/dd/mm/yy)
  - Support RTC to wake up system from Deep Sleep mode
- **ADC**
  - 12-bit SAR-type ADC with 7 channels, 12 bits, and 1 Msps sampling rate
- **Voltage comparator (VC)/Low-voltage detector (LVD)**
- **Hardware CRC-16 module**
- **Working conditions**
  - Wide supply voltage range: 2.5V-5.5V
  - Wide working frequency: up to 24 MHz
  - Working temperature: -40°C to +85°C
- **16-byte unique ID (UID) for chip**
- **Development tool**
  - Full-featured embedded debugging solution
  - In-system programming (ISP) scheme
- **Package: TSSOP20, QFN20**

1 Introduction

The CX32L003 microcontroller incorporates the 32-bit ARM® Cortex®-M0+ core with ultra-low power consumption and low pin count. It can operate at a wide range of working voltage (2.5V-5.5V) and a frequency up to 24 MHz. An embedded Flash of 32K/64K bytes and a SRAM of 4K bytes are built in, and a great number of peripheral such as 12-bit 1 Msps high-precision SAR-type ADC, RTC, comparator, multi-channel UART, SPI, I2C and PWM are integrated, making it a highly-integrated product with strong anti-interference and high reliability.

The CX32L003 series is capable of operating at a wide voltage working range with low power consumption and low standby current. Moreover, it features highly-integrated peripheral interfaces and fast wake-up, showing high operating efficiency and high cost performance. The product can be widely applied in:

home appliance, charger, remote controller, electronic cigarette, gas alarm, data display instrument, temperature controller, recorder, motor drive, intelligent door lock, intelligent sensor, intelligent home, smart city, etc.

	CX32L003F6	**CX32L003F8**
Number of pins	20	
GPIO general pin	16	
External interrupt	16	
Advanced-control timer (TIM1)	1	
General-purpose timer (TIM2)	1	
Programmable Counter Array (PCA)	1	
TIM10/11	2	
Number of A/D channels	7	
Flash (K byte)	32	64
SRAM (K byte)	4	
UART	2	
LPUART	1	
SPI	1	
I2C	1	
IWDG	1	
WWDG	1	
1-WIRE	1	
CRC16	1	
Buzzer	1	
AWK	1	
RTC	1	
LVD/VC	Support	
CPU frequency	ARM® Cortex®-M0+ 24 MHz (maximum)	
Voltage range	2.5~5.5V	
Temperature range	-40~85°C	
Flash protection	Support	
Package	TSSOP20, QFN20	

2 Product function overview

A brief description about the functions and peripheral basic characteristics of CX32L003 series products will be given in the chapters below.

2.1 32-bit Cortex®-M0+ core

ARM® Cortex®-M0+ processor is the latest-generation embedded 32-bit RISC processor. It features less pins, lower power consumption, advanced computing performance and interrupt system response, enabling a low-cost platform for MCU realization. The Cortex®-M0+ processor fully supports Keil and IAR IDE. It includes a hardware debug circuit that supports the 2-pin SWD debug interface.

Cortex®-M0+ features:

Instruction set	Thumb / Thumb-2
Pipeline	2-stage pipeline
CoreMark/MHz	2.46
DMIPS/MHz	0.95
Interrupt	32 interrupt sources
Interrupt priority	Configurable 4-level interrupt priority
Enhanced instruction	Single cycle 32-bit multiplier
Debugging interface	Support SWD 2-wire debugging interface, 4 hard break points, and 2 watch points.

2.2 Memory

2.2.1 Embedded flash memory (Flash)

Embedded flash memory (Flash) is used for storing programs and data. With a built-in fully-integrated Flash controller, no external high voltage input is required, and high voltage generated by the fully built-in circuits is used for programming. ISP function is supported.

- CX32L003F8 series supports up to 64K bytes.
- CX32L003F6 series supports up to 32K bytes.

2.2.2 Built-in SRAM

4K-byte built-in SRAM.

2.3 Clock system

An external high-frequency crystal oscillator HXT with a frequency of 4M~24 MHz

An external low-frequency crystal oscillator LXT with a frequency of 32.768 KHz

An external high-frequency crystal oscillator HIRC with a frequency of 4M~24 MHz

An internal low-frequency clock LIRC with a frequency of 32.768 KHz/38.4 KHz

2.4 Operating mode

CX32L003 supports 3 operating modes:

1. Active mode: CPU runs, and peripheral function modules run.
2. Sleep mode: CPU stops running, and peripheral function modules run.
3. Deep Sleep mode: CPU stops running, the system main clock is turned off, and the

low-power function modules run.

The operating mode can be selected through software. In Sleep mode, CPU clock is off, and other parts can still work. Interrupt can be used to wake up CPU. In Deep Sleep mode, the system main clock is off, and most modules stop running. The system is working with built-in 38.4 KHz/32.768 KHz low-speed clock. RTC interrupt, AWK interrupt or external interrupt can be used to wake up the chip. In active operating mode, clock frequency divider can be used or some unnecessary module clocks can be stopped for flexible switch of power consumption and performance.

2.5 Interrupt controller (NVIC)

Cortex®-M0+ processor has a built-in nested vectored interrupt controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs. With four interrupt priorities, it can handle complex logic for real-time control and interrupt handling.

For details, refer to “ARM® Cortex®-M0+ Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

There are 32 interrupt sources, as shown in Table 2-1 Interrupt source:

Table 2-1 Interrupt source

External interrupt number (IRQ#)	Interrupt source	Introduction	Sleep mode wake up	Deep Sleep mode wake up	Vector address
0	GPIO_PA	GPIOA interrupt	Y	Y	0x0000 0040
1	GPIO_PB	GPIOB interrupt	Y	Y	0x0000 0044
2	GPIO_PC	GPIOC interrupt	Y	Y	0x0000 0048
3	GPIO_PD	GPIOD interrupt	Y	Y	0x0000 004C
4	Flash	Flash interrupt	N	N	0x0000 0050
5	Reserved	-	-	-	0x0000 0054
6	UART0	UART0 interrupt	Y	N	0x0000 0058
7	UART1	UART1 interrupt	Y	N	0x0000 005C
8	LPUART	LPUART interrupt	Y	Y	0x0000 0060
9	Reserved	-	-	-	0x0000 0064
10	SPI	SPI interrupt	Y	N	0x0000 0068
11	Reserved	-	-	-	0x0000 006C
12	I2C	I2C interrupt	Y	N	0x0000 0070
13	Reserved	-	-	-	0x0000 006C
14	TIM10	TIM10 interrupt	Y	N	0x0000 0078
15	TIM11	TIM11 interrupt	Y	N	0x0000 007C
16	LPTIM	LPTIM interrupt	Y	Y	0x0000 0080
17	Reserved	-	-	-	0x0000 007C
18	TIM1	TIM1 interrupt	Y	N	0x0000 0088
19	TIM2	TIM2 interrupt	Y	N	0x0000 008C
20	Reserved	-	-	-	0x0000 0088
21	PCA	PCA interrupt	Y	N	0x0000 0094
22	WWDG	WWDG interrupt	Y	N	0x0000 0098
23	IWDG	IWDG interrupt	Y	Y	0x0000 009C
24	ADC	ADC interrupt	Y	N	0x0000 00A0
25	LVD	LVD interrupt	Y	Y	0x0000 00A4
26	VC	VC interrupt	Y	Y	0x0000 00A8
27	Reserved	-	-	-	0x0000 00A4
28	AWK	AWK interrupt	Y	Y	0x0000 00B0
29	OWIRE	1-WIRE interrupt	Y	N	0x0000 00B4
30	RTC	RTC interrupt	Y	Y	0x0000 00B8
31	CLKTRIM	CLKTRIM interrupt	Y	Y[Note]	0x0000 00BC

Note: Only when internal low-speed monitoring for external low-speed clock function is selected, the wake-up can work.

2.6 Reset controller

The product has 9 reset signal sources; each reset signal can reset CPU, and most registers will be reset again; the program counter (PC) will be reset and point to the reset address (0x0000 0000).

No.	Interrupt source
1	Power-on/power-down reset
2	External Reset Pin reset
3	IWDG reset
4	WWDG reset
5	System software reset
6	Under-voltage (LVD) reset
7	LOCKUP reset
8	Register CPURST reset
9	Register MCURST reset

2.7 General IO port (GPIO)

Up to 16 GPIO ports are available, and some GPIO ports are multiplexed with analog ports. Each port is controlled by an independent control register bit. It supports edge-triggered interrupts and level-triggered interrupts to wake up the MCU to active mode from a variety of low power modes. It also supports CMOS push-pull output and Open-Drain output. It has built-in pull-up resistor, pull-down resistor with Schmitt trigger input filtering. The output drive capability is configurable and supports up to 12 mA current drive capability. And 16 general IOs support external asynchronous interrupts.

2.8 Timer and watchdog

CX32L003 product comprises 1 advanced-control timer, 1 general-purpose timer, 1 programmable counter array, 2 basic timers, 1 low-power basic timer, 1 system window watchdog timer, 1 independent watchdog timer, and 1 SysTick timer.

The table below compares the features of advanced-control timer, general-purpose timer, and basic timer.

Table 2-2 Timer features

Timer type	Name	Counter bit width	Prescale coefficient	Counting direction	PWM output	Capture/ compare channel	Complementary output
Advanced	TIM1	16-bit	1/2/4/8/16/64/256/1024	Up, down, up/down	Yes	4	3 pairs
General	TIM2	16-bit	1/2/4/8/16/64/256/1024	Up, down, up/down	Yes	4	None
PCA	PCA	16-bit	2/4/8/16/32	Up	Yes	5	None
Low power	LPTIM	16-bit	None	Up	None	None	None
Basic	TIM10	16/32-bit	1/2/4/8/16/32/64/128	Up	None	None	None
	TIM11	16/32-bit	1/2/4/8/16/32/64/128	Up	None	None	None

2.8.1 Advanced-control timer (TIM1)

One advanced-control timer (TIM1) can be seen as a three-phase PWM generator distributed to 6 channels. It has complementary PWM outputs with dead time insert. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- Generating PWM (edge or center-aligned modes)
- When the single-pulse output is configured as a 16-bit standard timer, it has the same functions with TIMx timer. When configured as a 16-bit PWM generator, it has full modulation capacity (0~100%).

In debug mode, the counter can be frozen and the PWM output is disabled, so as to turn off the switches controlled these outputs. Many features are the same as those in the general-purpose TIM timer, and the internal architectures are same. Therefore, the advanced-control timer can work together with other TIM timers through timer link function for synchronization or event chaining.

2.8.2 General-purpose timer (TIM2)

The general-purpose timer (TIM2) has a 16-bit auto-load up/down counter, one 16-bit prescaler and 4 independent channels. Each channel can be used for input capture, output compare, PWM and one pulse mode output. It can work with other advanced-control timers via the timer link feature for synchronization or event chaining. The counter can be frozen in debug mode. Any standard timer can be used for generating PWM output.

2.8.3 Programmable counter array (PCA)

PCA (programmable counter array) supports up to five 16-bit capture/compare modules. The timer/counter can be used for the capture/compare function of a general clock counter/event counter. Each channel of PCA can be independently programmed to provide input capture/output compare, or pulse width modulation.

2.8.4 Low-power timer (LPTIM)

The low-power timer is 1 asynchronous 16-bit optional timer. The timing/counting is also available through internal low-speed LIRC or external low-speed crystal oscillator after the system clock is turned off. Wake up the system in low-power mode by interrupt.

2.8.5 Basic timer (TIM10/TIM11)

The basic timer has two 16/32-bit optional timers TIM10/TIM11. The functions of TIM10/TIM11 are the same, and both are synchronous timer/counter. The auto reload mode and non-auto reload mode can be selected. TIM10/TIM11 can count external pulses or realize system timing.

2.8.6 Independent watchdog (IWDG)

Independent watchdog is a 20-bit down counter. It is clocked by an internal independent LIRC; as the internal LIRC is independent of the main clock, it can operate in stop and standby modes. It can be used either as a watchdog to reset devices when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

2.8.7 System window watchdog (WWDG)

The system window watchdog is based on an 8-bit down counter, and supports 20-bit prescale.

Its action clock is provided by APB clock (PCLK). It can be seen as a watchdog to reset devices when a system problem occurs. It has an early-warning interrupt capability, and its counter can be frozen in debug mode.

2.8.8 SysTick timer (SYST)

This timer is dedicated to real-time operating systems, but it can also be used as a standard down counter. Its features are as follows:

- 24-bit down counter
- Auto-reload function
- Generate maskable system interrupt when the counter reaches 0
- Programmable clock source (HCLK or HCLK/4)

2.9 Real time clock (RTC)

- Support RTC counting (second/minute/hour) and calendar function (dd/mm/yy)
- Support alarm register (second/minute/hour/dd/mm/yy)
- RTC can wake up the system from Sleep mode.

2.10 Universal asynchronous receiver/transmitter (UART0/UART1)

2-channel universal asynchronous receiver/transmitter

2.11 Low power universal asynchronous receiver/transmitter (LPUART)

1-channel asynchronous receiver/transmitter that can work in low-power mode

2.12 Serial peripheral interface (SPI)

The 1-channel serial peripheral interface supports master and slave modes.

2.13 I^{2}C interface (I2C)

The 1-channel I2C interface supports master and slave modes. A serial synchronous clock is adopted, enabling data transmission between devices at different rates. The maximum speed of serial 8-bit dual-direction data transmission is up to 1 Mbps.

2.14 One-Wire interface (OWIRE)

Support One-Wire bus protocol.

2.15 Buzzer

The buzzer module can generate a buzzing signal at 1 KHz, 2 KHz and 4 KHz on the BEEP pin for driving external buzzers.

Function multiplex output is available between 2 basic timers TIM10/TIM11 and 1 LPTIM, providing programmable drive frequency for buzzer. Complementary output is supported, and no additional transistors are required.

2.16 Automatic wake-up timer (AWK)

AWK provides an internal wake-up time benchmark when MCU enters the low-power mode. The time benchmark clock is provided by internal low-speed RC oscillator clock (LIRC) or prescale

HXT crystal oscillator clock.

2.17 Clock calibration/monitoring module (CLKTRIM)

It is built in with a clock calibration circuit. The internal RC clock can be calibrated by an external precise oscillator clock. Or, the internal RC clock can be used to check whether the external crystal oscillator clock is normal.

2.18 Unique ID (UID)

Each chip has a unique 16-byte device identification number during ex-factory, including wafer lot information and chip coordinate information. ID address: 0x180000F0-0x180000FF.

2.19 Cyclic redundancy check (CRC) calculation unit

Conform to the multiple-term formula: $F(x)= X^{16} + X^{12} + X^5 + 1$ as situated in ISO/IEC13239

2.20 Analog/digital converter (ADC)

The 12-bit successive approximation analog-to-digital converter is monotonous and does not lose code. It has a sampling rate of 1 Msps when operating at a 16 MHz ADC clock. The reference voltage can be selected from power voltage. There are 7 external channels for single, scan, and cyclic conversion. In scan/cyclic mode, automatic conversion is available in a group of selected analog input.

- Input voltage range: 0 to VDD
- Conversion cycle: 16/20 clock cycles
- ADC sampling can be triggered from external terminal, internal TIM1, TIM2, TIM10/TIM11, VC and other modules.
- Interrupt after end of sampling (EOC)

2.21 Low-voltage detector (LVD)

Detect the power supply voltage or pin voltage of the chip. It has 8-speed voltage monitoring value (2.5-4.4V). An asynchronous interrupt or reset can be generated based on the rising/falling edge. It also has hardware hysteresis circuit and configurable software anti-shake function.

2.22 Voltage comparator (VC)

Chip pin voltage monitoring/comparing circuit. There are 3 configurable positive/negative external input channels with 1 internal BGR 2.5V reference voltage. VC output can be used for timers TIM1, TIM10/TIM11, LPTimer and PCA capture, gate control, and external counting. Asynchronous interrupt is generated based on rising/falling edge. Wake up MCU in low-power mode. The software anti-shake function is configurable.

2.23 Embedded debugging system

The embedded debugging solution provides a full-featured real-time debugger with standard and mature Keil/IAR debugging development software. It supports 4 hard break points and multiple soft break points.

2.24 Encrypted embedded debug (DBG)

This encrypted embedded debugging solution provides a full-featured real-time debugger. For details, refer to related chapters in the User Manual.

3 System and memory profile

3.1 System architecture

Main system composition:

- 1 AHB bus system Master:
  - Cortex®-M0+ core
- 6 AHB bus Slaves
  - Internal SRAM
  - Internal Flash
  - AHB to APB Bridge, including all APB interface peripherals
  - GPIO interface
  - RCC module
  - CRC and other AHB interface modules

For system chart, refer to Fig 3-1 System Block Diagram:

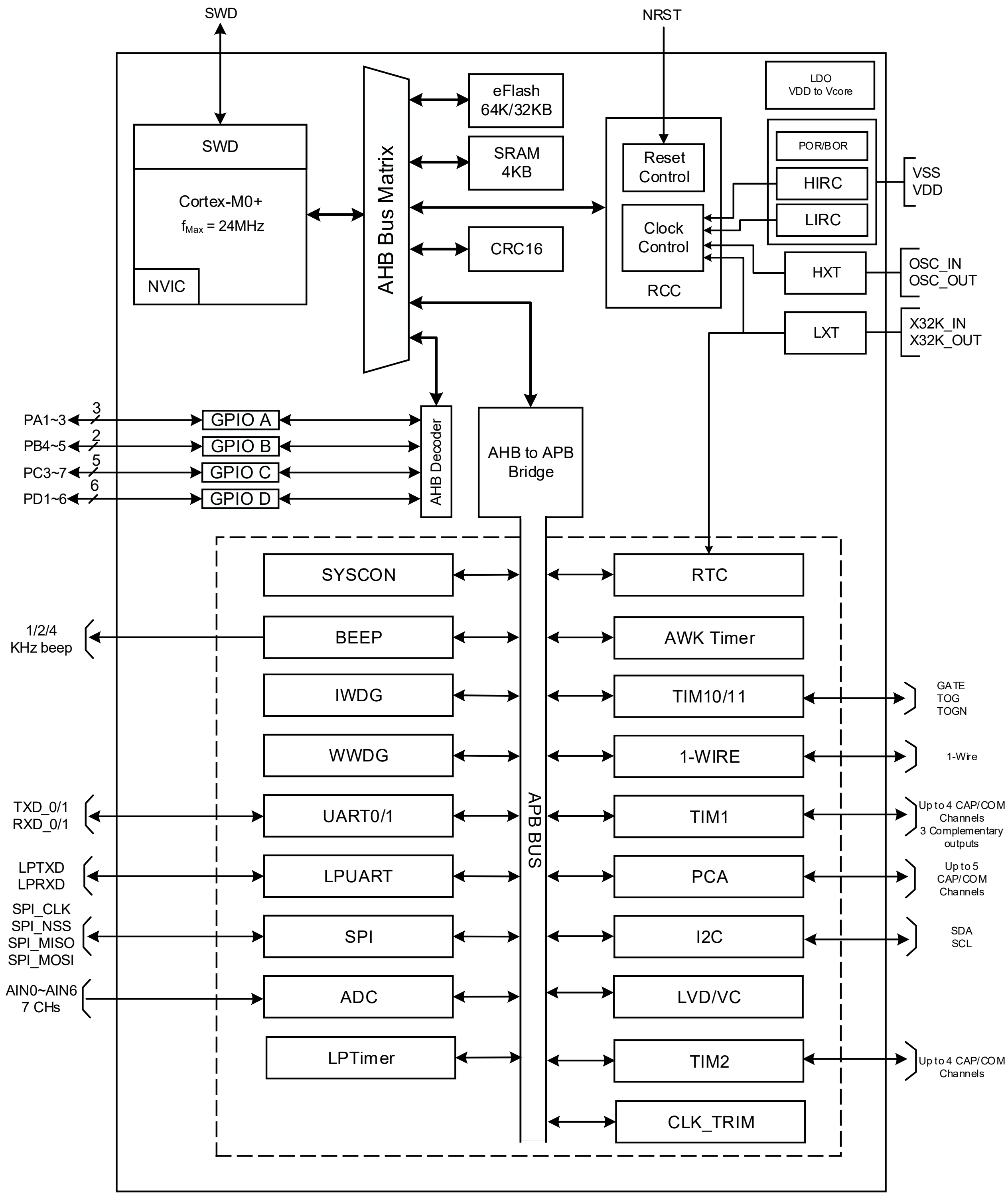


Fig 3-1 System Block Diagram

3.2 Memory mapping

The system address size is 4 GB in total, including program storage space, data storage space, periphery module register, I/O port, etc. The data adopts little endpoint mode, that is, the high byte of data is stored in high address of the memory, while the low byte of data is stored in low address of the memory. The division of space of the entire system address is shown in. Fig. 3-2 below:

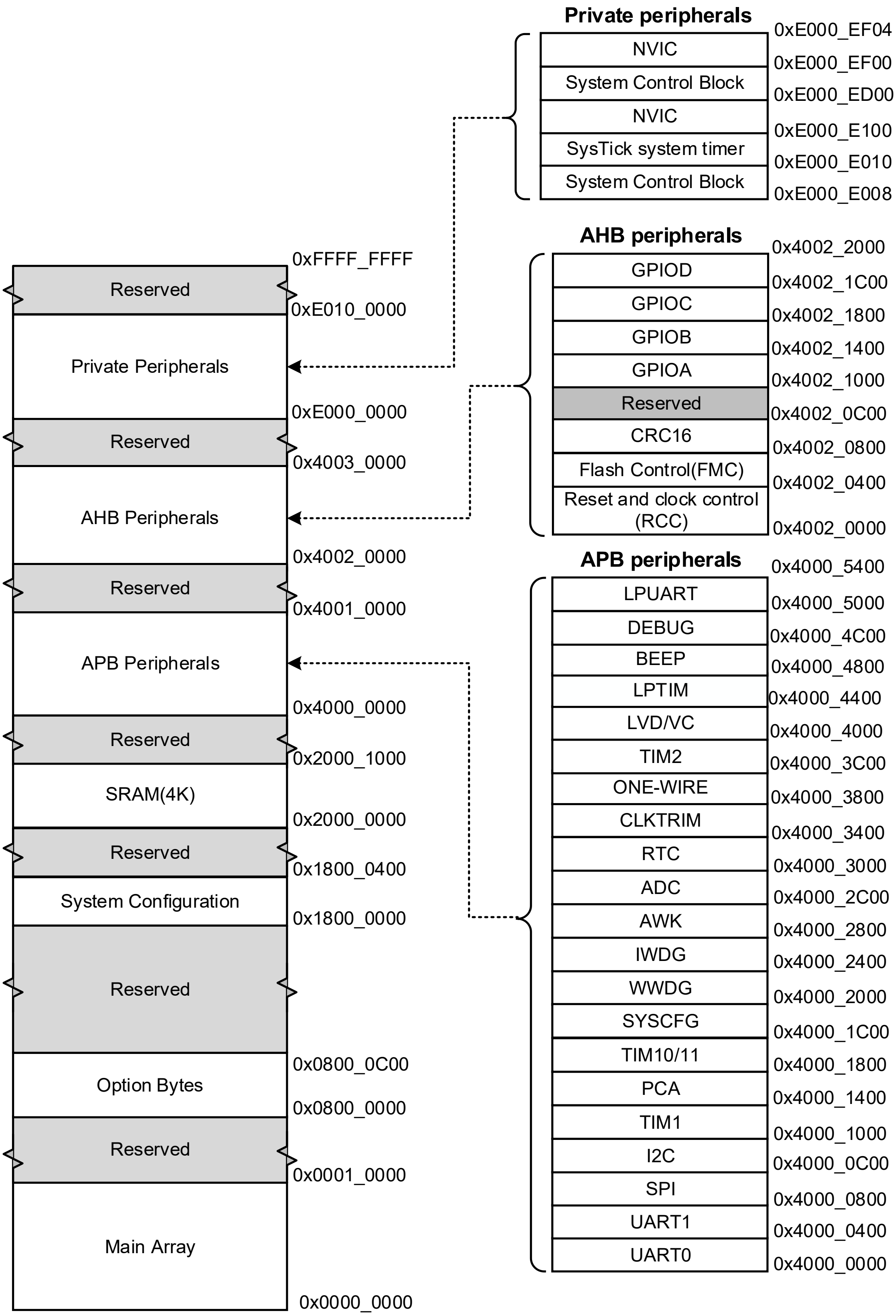


Fig. 3-2 Memory mapping

3.3 Storage space and module address

Table 3-1 below describes address space and periphery information for each module in CX32L003 device.

Table 3-1 CX32L003 memory mapping and peripheral register addressing

Bus	Periphery address	Size (Bytes)	Module
	0xE000_0000 - 0xE00F_FFFF	1M	Coretex-M0+ peripheral
	0x4003_0000 - 0xDFFF_FFFF		Reserved
AHB	0x4002_1000 - 0x4002_1FFF	1K	GPIOD
	0x4002_1000 - 0x4002_1BFF	1K	GPIOC
	0x4002_1000 - 0x4002_17FF	1K	GPIOB
	0x4002_1000 - 0x4002_13FF	1K	GPIOA
	0x4002_0C00 - 0x4002_0FFF	1K	Reserved
	0x4002_0800 - 0x4002_0BFF	1K	CRC16
	0x4002_0400 - 0x4002_07FF	1K	FMC
	0x4002_0000 - 0x4002_03FF	1K	RCC
	0x4000_5400 - 0x4001_FFFF		Reserved
APB	0x4000_5000 - 0x4000_53FF	1K	LPUART
	0x4000_4C00 - 0x4000_4FFF	1K	DEBUG
	0x4000_4800 - 0x4000_4BFF	1K	BEEP
	0x4000_4400 - 0x4000_47FF	1K	LPTIM
	0x4000_4000 - 0x4000_43FF	1K	LVD/VC
	0x4000_3C00 - 0x4000_3FFF	1K	TIM2
	0x4000_3800 - 0x4000_3BFF	1K	OWIER
	0x4000_3400 - 0x4000_37FF	1K	CLKTRIM
	0x4000_3000 - 0x4000_33FF	1K	RTC
	0x4000_2C00 - 0x4000_2FFF	1K	ADC
	0x4000_2800 - 0x4000_2BFF	1K	AWK
	0x4000_2400 - 0x4000_27FF	1K	IWDT
	0x4000_2000 - 0x4000_23FF	1K	WWDT
	0x4000_1C00 - 0x4000_1FFF	1K	SYSCON
	0x4000_1800 - 0x4000_1BFF	1K	TIM10/11
	0x4000_1400 - 0x4000_17FF	1K	PCA
	0x4000_1000 - 0x4000_13FF	1K	TIM1
	0x4000_0C00 - 0x4000_0FFF	1K	I2C
	0x4000_0800 - 0x4000_0BFF	1K	SPI
	0x4000_0400 - 0x4000_07FF	1K	UART1
	0x4000_0000 - 0x4000_03FF	1K	UART0
AHB	0x2000_1000 - 0x3FFF_FFFF		Reserved
	0x2000_0000 - 0x2000_0FFF	4K	SRAM
	0x1800_0100 - 0x1FFF_FFFF		Reserved
	0x1800_0000 - 0x1800_00FF	256	System Configuration
	0x0800_0200 - 0x17FF_FFFF		Reserved
	0x0800_0000 - 0x0800_01FF	512	Option Bytes
	0x0001_0000 - 0x07FF_FFFF		Reserved
	0x0000_0000 - 0x0000_FFFF	64K	Main Array (Flash)

4 Pin configuration and function description

4.1 CX32L003 TSSOP20/QFN20 configuration

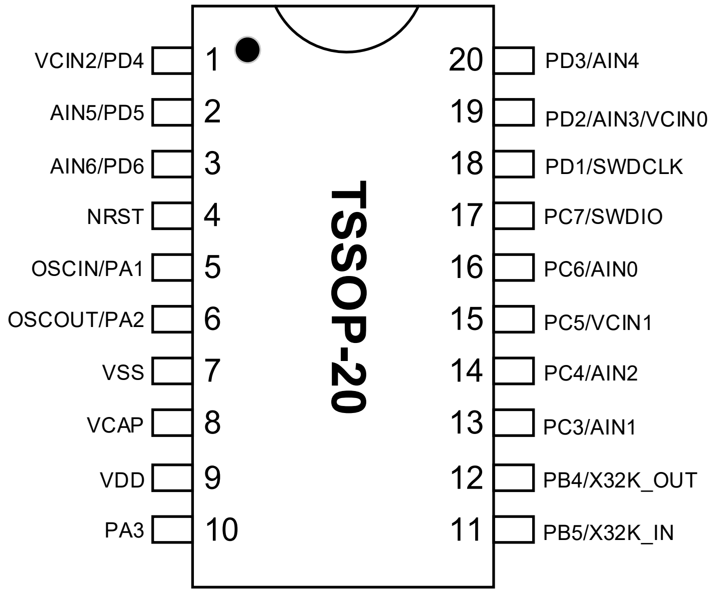


Fig. 4-1 TSSOP20 pin configuration

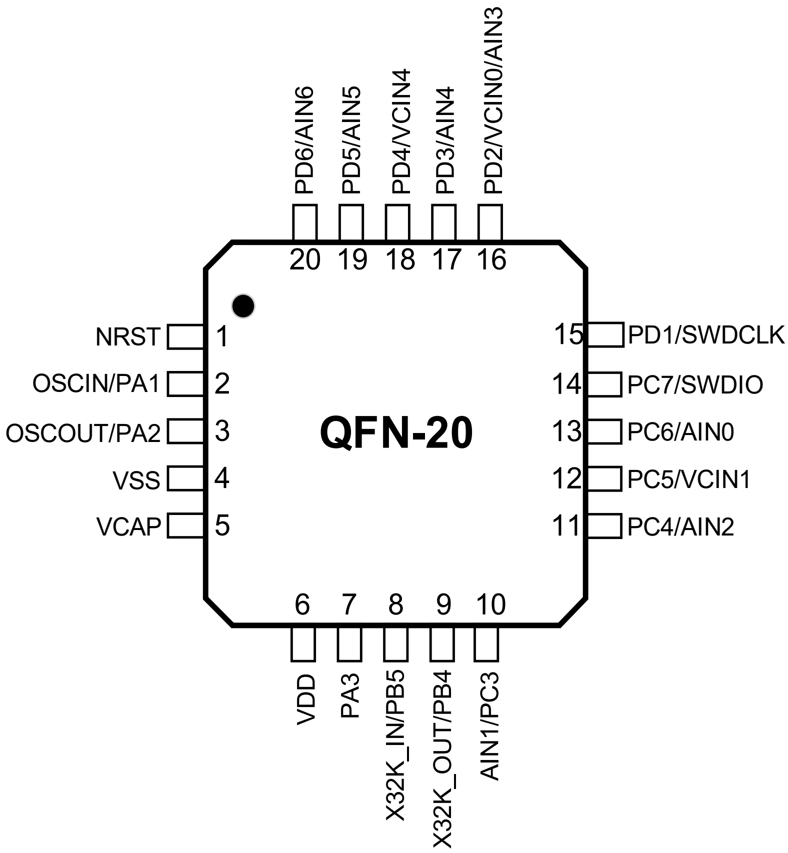


Fig. 4-2 QFN20 pin configuration

4.2 CX32L003 pin multiplex

Table 4-1 pin function multiplex

Encapsulation			GPIOx_AFR[i+3:i]									
TSSOP20	QFPN20	Config	0	1	2	3	4	5	6	7	8	F
1	18		PD4	TIM1_CH1	PCA_CH0	RTC_1HZ	TIM10_TOG	UART0_TXD	TIM10_EXT	BEEP	TIM2_CH1	VCIN2
2	19		PD5	TIM1_CH1N	PCA_CH4	SPI_MISO	I2C_SCL	UART1_TXD	TIM10_GATE	UART0_TXD	TIM2_CH4	AIN5
3	20		PD6	TIM1_CH2	PCA_CH3	SPI_MOSI	I2C_SDA	UART1_RXD	LPTIM_EXT	UART0_RXD	TIM2_CH2	AIN6
4	1	NRST										
5	2	OSC_IN	PA1	TIM1_CH2N		SPI_CLK	I2C_SDA	UART0_RXD	TIM10_TOG	UART1_RXD		
6	3	OSC_OUT	PA2	TIM1_CH3		SPI_NSS	I2C_SCL	UART0_TXD	TIM10_TOGN	UART1_TXD	TIM2_CH2	
7	4	VSS										
8	5	VCAP										
9	6	VDD										
10	7		PA3	TIM1_CH3N	PCA_CH2	SPI_NSS	RTC_1HZ	LPUART_RXD	PCA_ECI	VC0_OUT	TIM2_CH3	
11	8	X32K_IN	PB5	TIM1_BKIN	PCA_CH4	SPI_CLK	I2C_SDA	UART0_RXD	TIM11_TOG	LVD_OUT	TIM2_CH1	
12	9	X32K_OUT	PB4	LPTIM_GATE	PCA_ECI	SPI_NSS	I2C_SCL	UART0_TXD	TIM11_TOGN			
13	10		PC3	TIM1_CH3	TIM1_CH1N		I2C_SDA	UART1_TXD	PCA_CH1	1-WIRE	TIM2_CH3	AIN1
14	11		PC4	TIM1_CH4	TIM1_CH2N		I2C_SCL	UART1_RXD	PCA_CH0	CLK_MCO	TIM2_CH4	AIN2
15	12		PC5	TIM1_BKIN	PCA_CH0	SPI_CLK		LPUART_TXD	TIM11_GATE	LVD_OUT	TIM2_CH1	VCIN1
16	13		PC6	TIM1_CH1	PCA_CH3	SPI_MOSI		LPUART_RXD	TIM11_EXT	CLK_MCO	TIM2_CH4	AIN0
17	14	SWDIO	PC7	TIM1_CH2	PCA_CH4	SPI_MISO		UART1_RXD	LIRC_OUT	LXT_OUT		
18	15	SWDCLK	PD1		PCA_ECI			UART1_TXD	HIRC_OUT	VC0_OUT		
19	16		PD2	TIM1_CH2	PCA_CH2	SPI_MISO	RTC_1HZ	LPUART_TXD	LPTIM_TOG	1-WIRE		AIN3/VCIN0
20	17		PD3	TIM1_CH3N	PCA_CH1	SPI_MOSI	HXT_OUT	UART0_RXD	LPTIM_TOGN		TIM2_CH2	AIN4

4.3 CX32L003 Pin function description

Pin No. (TSSOP-20)	Pin No. (QFN-20)	Pin Name	Pin Type	Description
1	18	PD4	PD4	PD4 general digital input/output pin
			TIM1_CH1	TIM1 PWM output 1
			PCA_CH0	PCA capture input/compare output 0
			RTC_1HZ	RTC 1HZ output
			TIM10_TOG	TIM10 flip output
			UART0_TX	UART0 TX
			TIM10_EXT	TIM10 external pulse input
			BEEP	BEEP output
			TIM2_CH1	TIM2 capture input/compare output 1
			VCIN2	Voltage comparator input channel 2
2	19	PD5	PD5	PD5 general digital input/output pin
			TIM1_CH1N	TIM1 PWM output 1 invert
			PCA_CH4	PCA capture input/compare output 4
			SPI_MISO	SPI module MISO (master input slave output) signal
			I2C_SCL	I^2C clock
			UART1_TX	UART1_TX
			TIM10_GATE	TIM10 gate control
			UART0_TX	UART0 TX
			TIM2_CH4	TIM2 capture input/compare output 4
			AIN5	ADC analog input channel 5
3	20	PD6	PD6	PD6 general digital input/output pin
			TIM1_CH2	TIM1 PWM output 2
			PCA_CH3	PCA capture input/compare output 3
			SPI_MOSI	SPI module MOSI (master output slave input) signal
			I2C_SDA	I^2C data
			UART1_RX	UART1 RX
			LPTIM_EXT	LPTIM external pulse input
			UART0_RX	UART0 RX
			TIM2_CH2	TIM2 capture input/compare output 2
			AIN6	ADC analog input channel 6
4	1	NRST	NRST	Reset input port, active low, chip reset
5	2	PA1	OSC_IN	External crystal oscillator input
			PA1	PA1 general digital input/output pin
			TIM1_CH2N	TIM1 PWM output 2 invert
			SPI_CLK	SPI module clock signal
			I2C_SDA	I^2C data
			UART0_RX	UART0 RX

Pin No. (TSSOP-20)	Pin No. (QFN-20)	Pin Name	Pin Type	Description
			TIM10_TOG	TIM10 flip output
			UART1_RX	UART1 RX
6	3	PA2	OSC_OUT	External crystal oscillator output
			PA2	PA2 general digital input/output pin
			TIM1_CH3	TIM1 PWM output 3
			SPI_NSS	SPI module slave chip selection signal
			I2C_SCL	I^2C clock
			UART0_TX	UART0 TX
			TIM10_TOGN	TIM10 flip invert output
			UART1_TX	UART1 TX
			TIM2_CH2	TIM2 capture input/compare output 2
7	4	VSS	GND	Chip ground
8	5	VCAP	Power	LDO core power supply output (only for internal circuits, and external circuit is connected to capacitance)
9	6	VDD	Power	Chip power supply
10	7	PA3	PA3	PA3 general digital input/output pin
			TIM1_CH3N	TIM1 PWM output 3 invert
			PCA_CH2	PCA capture input/compare output 2
			SPI_NSS	SPI module slave chip selection signal
			RTC_1HZ	RTC 1HZ output
			LPUART_RX	LPUART RX
			PCA_ECI	PCA external clock
			VC0_OUT	Voltage comparator 0 output
			TIM2_CH3	TIM2 capture input/compare output 3
11	8	PB5	X32K_IN	External 32K crystal oscillator input
			PB5	PB5 general digital input/output pin
			TIM1_BKIN	TIM1 break signal input
			PCA_CH4	PCA capture input/compare output 4
			SPI_CLK	SPI module clock signal
			I2C_SDA	I^2C data
			UART0_RX	UART0 RX
			TIM11_TOG	TIM11 flip output
			LVD_OUT	Low-voltage detection comparator output
			TIM2_CH1	TIM2 capture input/compare output 1
12	9	PB4	X32K_OUT	External 32K crystal oscillator output
			PB4	PB4 general digital input/output pin
			LPTIM_GATE	LPTIM gate control
			PCA_ECI	PCA external clock
			SPI_NSS	SPI module slave chip selection signal
			I2C_SCL	I^2C clock

Pin No. (TSSOP-20)	Pin No. (QFN-20)	Pin Name	Pin Type	Description
			UART0_TX	UART0 TX
			TIM11_TOGN	TIM11 flip invert output
13	10	PC3	PC3	PC3 general digital input/output pin
			TIM1_CH3	TIM1 PWM output 3
			TIM1_CH1N	TIM1 PWM output 1 invert
			I2C_SDA	I^2C data
			UART1_TX	UART1 TX
			PCA_CH1	PCA capture input/compare output 1
			1-WIRE	1-wire input/output
			TIM2_CH3	TIM2 capture input/compare output 3
			AIN1	ADC analog input channel 1
14	11	PC4	PC4	PC4 general digital input/output pin
			TIM1_CH4	TIM1 PWM output 4
			TIM1_CH2N	TIM1 PWM output 2 invert
			I2C_SCL	I^2C clock
			UART1_RX	UART1 RX
			PCA_CH0	PCA capture input/compare output 0
			CLK_MCO	CPU clock output
			TIM2_CH4	TIM2 capture input/compare output 4
			AIN2	ADC analog input channel 2
15	12	PC5	PC5	PC5 general digital input/output pin
			TIM1_BKIN	TIM1 break signal input
			PCA_CH0	PCA capture input/compare output 0
			SPI_CLK	SPI module clock signal
			LPUART_TX	LPUART TX
			TIM11_GATE	TIM11 gate control
			LVD_OUT	Low-voltage detection comparator output
			TIM2_CH1	TIM2 capture input/compare output 1
			VCIN1	Analog input
16	13	PC6	PC6	PC6 general digital input/output pin
			TIM1_CH1	TIM1 PWM output 1
			PCA_CH3	PCA capture input/compare output 3
			SPI_MOSI	SPI module MOSI (master output slave input) signal
			LPUART_RX	LPUART RX
			TIM11_EXT	TIM11 external pulse input
			CLK_MCO	CPU clock output
			TIM2_CH4	TIM2 capture input/compare output 4
			AIN0	ADC analog input channel 0
17	14	PC7	SWDIO	SWD IO
			PC7	PC7 general digital input/output pin

Pin No. (TSSOP-20)	Pin No. (QFN-20)	Pin Name	Pin Type	Description
			TIM1_CH2	TIM1 PWM output 2
			PCA_CH4	PCA capture input/compare output 4
			SPI_MISO	SPI module MISO (master input slave output) signal
			UART1_RX	UART1 RX
			LIRC_OUT	38.4 KHz output of internal low-frequency RC clock
			X32K_OUT	External low-frequency crystal oscillator output
18	15	PD1	SWDCLK	SWD clock
			PD1	PD1 general digital input/output pin
			PCA_ECI	PCA external clock
			UART1_TX	UART1 TX
			HIRC_OUT	24 MHZ output of internal high-frequency RC clock
			VC0_OUT	Voltage comparator 0 output
19	16	PD2	PD2	PD2 general digital input/output pin
			TIM1_CH2	TIM1 PWM output 2
			PCA_CH2	PCA capture input/compare output 2
			SPI_MISO	SPI module MISO (master input slave output) signal
			RTC_1HZ	RTC 1HZ output
			LPUART_TX	LPUART TX
			LPTIM_TOG	LPTIM flip output
			1-WIRE	1-wire input/output
			VCIN0	Voltage comparator input channel 0
			AIN3	ADC analog input channel 3
20	17	PD3	PD3	PD3 general digital input/output pin
			TIM1_CH3N	TIM1 PWM output 3 invert
			PCA_CH1	PCA capture input/compare output 1
			SPI_MOSI	SPI module MOSI (master output slave input) signal
			HXT_OUT	External-connected high-frequency crystal oscillator output
			UART0_RX	UART0 RX
			LPTIM_TOGN	LPTIM flip invert output
			TIM2_CH2	TIM2 capture input/compare output 2
			AIN4	ADC analog input channel 4

5 Electrical characteristics

5.1 Test conditions

Unless otherwise stated, all voltages are based on VSS.

5.1.1 Minimum and maximum values

Unless otherwise specified, in the tests performed for 100% products under T_A = 25°C and T_A = $T_{op,Max}$ (where, $T_{op,Max}$ depends on the corresponding temperature range of selected Part Number) on the production line, all minimum and maximum values will be guaranteed under the worst ambient temperature, supply voltage and clock frequency.

In the comment under each table, describe the data obtained from comprehensive assessment, design simulation and/or process performance. No test is made on the production line; on the basis of comprehensive assessment, the minimum and maximum values are obtained from the average value plus/minus three times of standard distribution (±3Σ) after sample test.

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25°C and VDD=3.3V (2.5V≤VDD≤5.5V). These data are only used for design guidance and are not tested.

Typical ADC accuracy value is obtained within all temperature range for a standard batch sampling, and the error of 95% products is less than or equal to the given value (average: ±2Σ).

5.2 Absolute maximum rating

Symbol	Parameter	Condition	Minimum value	Typical values	Maximum value	Unit
VDD	Supply voltage		2.5		5.5	V
V_{IO}	IO voltage		-0.3		VDD+0.3	V
T_{STG}	Storage temperature		-40	25	150	°C
T_{OP}	Working temperature		-40	25	85	°C
F_{CPU}	CPU working frequency		32.768K	4M	24M	Hz
$V_{ESD, HBM}$	Refer to 5.12					
$V_{ESD, CDM}$	Refer to 5.12					
$V_{ESD, MM}$	Refer to 5.12					

Note:

1. Temperature test method: Test high temperature of 85°C during the CP stage. The chip level tests at low temperature of -40°C and high temperature of 85°C are only conducted in lab and during Production Quality Qualification tests.
2. Frequency test method: Test 24 MHz frequency during the CP stage. The final test only focuses on the defects of encapsulation process

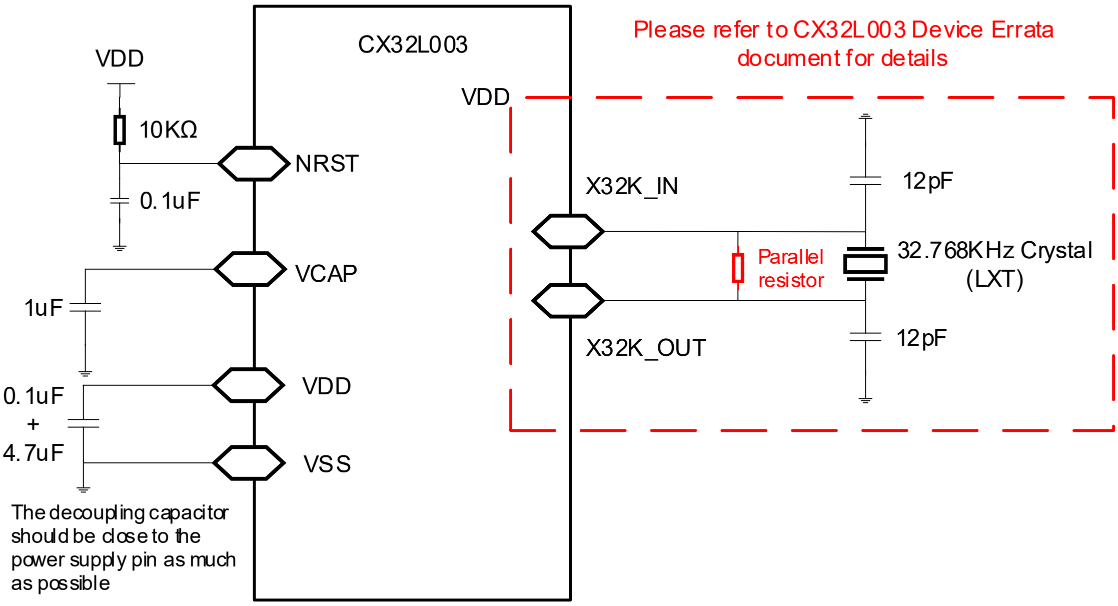
5.3 Recommended working conditions

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit	Reference
VDD	Supply voltage	-	2.5	5.5	V	
C_s	VCAP capacitance	-	0.47	2.2	μF	Recommended value: 1.0 μF
T_{OP}	Working temperature	-	-40	85	°C	

Note:

1. Recommended working conditions are designed to ensure normal work of semiconductor chip. In recommended working conditions, all specifications of electrical characteristics can be guaranteed. Make sure to use the semiconductor chip under recommended working conditions. Otherwise, it may affect the reliability of the semiconductor.
2. The Company provides no guarantee for items, usage conditions or logic combination usage not covered in this Data Manual. If the user considers using this chip beyond conditions listed herein, please contact sales representatives in advance.

5.4 Typical application block diagram



5.5 DC characteristics

5.5.1 Supply current characteristics

Symbol	Parameter	Condition			Typical values	Maximum value	Unit
I_{DD} (Run Mode in RAM)	All Peripherals clock OFF, Run while(1) in RAM	V_{core} =1.2V VDD=2.5V-5.5V	Clock source: HIRC	4M	157.20	171.00	µA
				8M	250.80	266.00	
				16M	427.80	444.00	
				24M	605.00	626.00	
I_{DD} (Run Mode in Flash)	All Peripherals clock ON, Run while(1) in Flash	V_{core} =1.2V VDD=2.5V-5.5V	Clock source: HIRC	4M	491.40	520.00	µA
				8M	915.20	968.00	
				16M	1751.00	1847.00	
				24M	2566.60	2691.00	
	All Peripherals clock OFF, Run while(1) in Flash	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: HIRC	4M	432.80	460.00	µA
				8M	799.40	848.00	
				16M	1519.00	1607.00	
				24M	2217.80	2334.00	
	All Peripherals clock ON, Run while(1) in Flash	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LXT 32.768KHz Driver=1	Ta=-40°C	26.48	30.00	
				Ta=25°C	28.00	30.00	µA
				Ta=50°C	28.40	31.00	
				Ta=85°C	31.21	34.06	
	All Peripherals clock OFF, Run while(1) in Flash	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LXT 32.768KHz Driver=1	Ta=-40°C	25.90	29.00	
				Ta=25°C	27.20	30.00	µA
				Ta=50°C	28.00	30.00	
				Ta=85°C	31.12	33.55	
I_{DD} (Sleep Mode)	All Peripherals clock ON	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: HIRC	4M	148.60	162.00	µA
				8M	236.40	251.00	
				16M	413.00	433.00	
				24M	588.00	616.00	
	All Peripherals clock OFF	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: HIRC	4M	90.40	102.00	µA
				8M	120.40	133.00	
				16M	180.00	195.00	
				24M	239.20	255.00	
	All Peripherals clock ON	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LXT 32.768KHz Driver=1	Ta=-40°C	24.70	28.00	
				Ta=25°C	26.00	28.00	µA
				Ta=50°C	26.80	29.00	
				Ta=85°C	29.24	32.00	
	All Peripherals clock OFF	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LXT 32.768KHz Driver=1	Ta=-40°C	24.25	27.00	
				Ta=25°C	25.60	28.00	µA
				Ta=50°C	26.20	28.00	
				Ta=85°C	28.99	31.00	
I_{DD} (DeepSleep	All Peripherals clock OFF, except	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LIRC	Ta=-40°C	0.89	1.03	µA
				Ta=25°C	1.06	1.20	

Symbol	Parameter	Condition			Typical values	Maximum value	Unit
Mode)	RTC, IWDG, LPTIM, AWK		32.768KHz	Ta=50°C	1.31	1.53	
				Ta=85°C	3.23	4.25	
	All Peripherals clock OFF, except RTC	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LIRC 32.768KHz	Ta=-40°C	0.87	1.03	µA
				Ta=25°C	1.03	1.18	
				Ta=50°C	1.34	1.63	
				Ta=85°C	3.49	5.22	
	All Peripherals clock OFF, except IWDG	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LIRC 32.768KHz	Ta=-40°C	0.88	1.06	µA
				Ta=25°C	1.02	1.14	
				Ta=50°C	1.28	1.50	
				Ta=85°C	3.13	3.88	
	All Peripherals clock OFF, except LPTIM	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LIRC 32.768KHz	Ta=-40°C	0.89	1.05	µA
				Ta=25°C	1.03	1.15	
				Ta=50°C	1.31	1.51	
				Ta=85°C	3.11	3.80	
	All Peripherals clock OFF, except AWK	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LIRC 32.768KHz	Ta=-40°C	0.86	0.99	µA
				Ta=25°C	0.99	1.10	
				Ta=50°C	1.28	1.48	
				Ta=85°C	3.07	3.77	
	All Peripherals clock OFF,	V_{core} =1.2V VDD =2.5V-5.5V		Ta=-40°C	0.90	1.47	µA
				Ta=25°C	1.02	1.15	
				Ta=50°C	1.30	1.84	
				Ta=85°C	3.09	3.81	

Note:

1. The data is based on the TT Wafer evaluation result, and is not tested in the production.
2. Unless otherwise specified, typical value (Typ) is measured under Ta = 25°C and VDD = 3.3V
3. Unless otherwise specified, maximum value (Max) is measured under Ta = -40°C~85°C and VDD = 2.5V~5.5V
4. When LXT 32.768 KHz is used, a 3 MΩ resistor is connected to the external crystal oscillator in parallel.

5.5.2 Power On Reset/Brown Out Reset

Symbol	Parameter	Condition	Minimum value	Typical values	Maximum value	Unit
V_{POR} V_{BOR}	POR release voltage (Power On Process) BOR detection voltage (Brown Out Process)		2.2	2.25	2.3	V

Note: Designed by design, and not tested in the production.

5.6 AC characteristics

5.6.1 Output characteristics -Ports PA, PB, PC, PD

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
V_{OH}	High level output voltage Source Current	Sourcing 4 mA, VDD = 3.3 V (see Note 1)	VDD-0.2		V
		Sourcing 6 mA, VDD = 3.3 V (see Note 2)	VDD-0.3		
V_{OL}	Low level output voltage Sink Current	Sinking 4 mA, VDD = 3.3 V (see Note 1)		VSS+0.2	V
		Sinking 6 mA, VDD = 3.3 V (see Note 2)		VSS+0.3	
V_{OHD}	High level output voltage Double Source Current	Sourcing 8 mA, VDD = 3.3 V (see Note 1)	VDD-0.2		V
		Sourcing 12 mA, VDD = 3.3 V (see Note 2)	VDD-0.3		
V_{OLD}	Low level output voltage Double Sink Current	Sinking 8 mA, VDD = 3.3 V (see Note 1)		VSS+0.2	V
		Sinking 12 mA, VDD = 3.3 V (see Note 2)		VSS+0.3	

Note:

1. The maximum total current, IOH(max) and IOL(max), for all outputs combined, should not exceed 40 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, IOH(max) and IOL(max), for all outputs combined, should not exceed 100 mA to satisfy the maximum specified voltage drop.
3. Obtained from comprehensive evaluation, and not tested in the production.

5.6.2 Input characteristics - Ports PA, PB, PC, PD

Symbol	Parameter	Condition	Minimum value	Typical values	Maximum value	Unit
V_{IT+}	Positive-going input threshold voltage	VDD=2.5	1.4			V
		VDD=3.3	1.8			V
		VDD=5.5	3			V
V_{IT-}	Negative-going input threshold voltage	VDD=2.5			0.9	V
		VDD=3.3			1.3	V
		VDD=5.5			2.4	V
V_{hys}	Input voltage hysteresis (VIT+ - VIT-)	VDD=2.5		0.5		V
		VDD=3.3		0.5		V
		VDD=5.5		0.6		V
$R_{pullhigh}$	Pullup Resistor	Pullup enable	40	50	60	Kohm
C_{input}	Input Capacitance			5		pf

Note: Obtained from comprehensive evaluation, and not tested in the production.

5.6.3 Port leakage characteristics - PA, PB, PC, PD

Symbol	Parameter	Condition	VDD	Maximum value	Unit
I_{lkg}	Leakage current	See Note 1, 2	2.5V / 3.6V	±50	nA

Notes:

1. The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.
3. Obtained from comprehensive evaluation, and not tested in the production.

5.6.4 Input sampling requirements for timer/counter

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
T(int)	External interrupt timing	External trigger signal for the interrupt flag(see Note 1)	30		ns
T(cap)	Timer Captuter timing	TIM1/TIM2 capture pulse width Fsystme =4MHz	0.5		μs
f_{EXT}	Timer clock frequency applied to pin	TIM1,TIM2,TIM10,TIM11 external clock input Fsystme =4MHz	0	$f_{TIMxCLK}/4$	MHz
T(PCA)	PCA clock frequency applied to pin	PCA external clock input Fsystme =4MHz	0	$f_{PCACLK}/4$	MHz

Note:

1. The external signal sets the interrupt flag every time the minimum t(int) parameters are met. It may be set even with trigger signals shorter than t(int).
2. Obtained from comprehensive evaluation, and not tested in the production.

5.6.5 Internal HIRC oscillator

Symbol	Parameter	Condition	Minimum value	Typical values	Maximum value	Unit
F_{MCLK}	Internal RC Oscillation frequency		4.0	4.0 8.0 16.0 24	24	MHz
T_{Mstart}(1)	Start-up time Not including software calibration	F_{MCLK}=4MHz	4.04	4.71	5.60	μs
		F_{MCLK}=8MHz	2.52	2.78	3.30	μs
		F_{MCLK}=16MHz	1.88	2.00	2.22	μs
		F_{MCLK}=24MHz	1.64	1.78	1.99	μs
I_{MCLK}	Current consumption	F_{MCLK}=4MHz	30	60	120	μA
		F_{MCLK}=8MHz	40	80	160	μA
		F_{MCLK}=16MHz	75	150	300	μA
		F_{MCLK}=24MHz	100	200	400	μA
DC_{MCLK}	Duty cycle		45	50	55	%
D_{evM}	Frequency Deviation	VDD = 2.5V ~ 5.5V Ta = -40°C ~ 85°C	-2.5		+2.5	%

Note: The data is based on the evaluation result, and is not tested in the production.

5.6.6 Internal LIRC oscillator

Symbol	Parameter	Condition	Minimum value	Typical values	Maximum value	Unit
F_{ACLK}	Internal RC Oscillation frequency		37.83 32.28	38.4 32.768	38.97 33.26	KHz
T_{Astart}(1)	Start-up time		68.21	74.74	80.00	μs
I_{ACLK}	Current consumption		0.2	0.25	0.35	μA
DC_{ACLK}	Duty cycle		45	50	55	%
D_{evA}	Frequency Deviation	VDD = 2.5V ~ 5.5V Ta = -40°C ~ 85°C	-2.5		+2.5	%

Note: The data is based on the evaluation result, and is not tested in the production.

5.6.7 External LXT crystal oscillator

Symbol	Parameter	Condition	Minimum value	Typical values	Maximum value	Unit
F_{SCLK}	Crystal frequency		32.75	32.768	32.78	KHz
ESR_{SCLK}	Supported crystal equivalent series resistance		40	65	85	KOhm
C_{SCLK}(1)	Supported crystal external external load range	There are two C_{SCLK} on 2 crystal pins respectively		12		pF
Idd(2)	Current consumption when stable	ESR=65KOhm C_{SCLK}=12pF	200	250	350	nA
DC_{SCLK}	Duty cycle		40	50	60	%
T_{start}(3)	Start-up time	ESR=65KOhm C_{SCLK}=12pF 40%~60% duty cycle reached		2		s

Note:

1. It is recommended to give reference values with crystal
2. RCC_LXTCR.LXTDRV = 0011, ESR = 65K
3. The data is based on the evaluation result, and is not tested in the production.

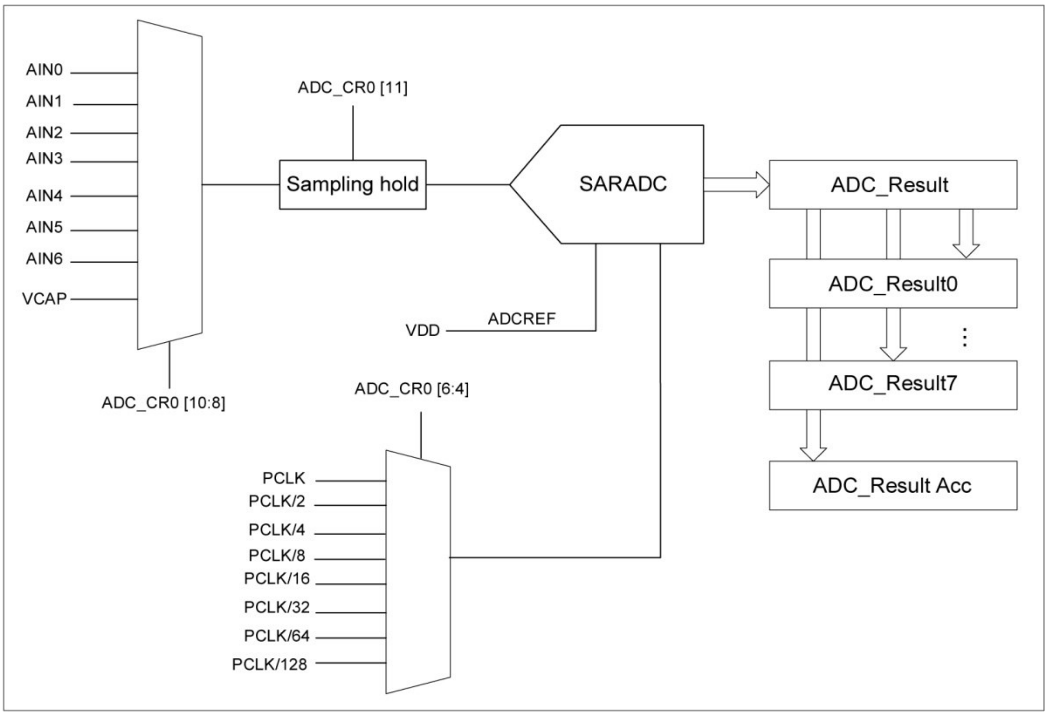
5.6.8 External HXT crystal oscillator

Symbol	Parameter	Condition	Minimum value	Typical values	Maximum value	Unit
F_{FCLK}	Crystal frequency		4	16	24	MHz
ESR_{FCLK}	Supported crystal equivalent series resistance		30	60	1500	Ohm
C_{FCLK}(1)	Supported crystal external external load range	There are 2 C_{FCLK} on 2 crystal pins individually		12		pF
Idd(2)	Current consumption	24MHz Xtal ESR=30Ohm C_{FCLK}=12pF		300		μA
DC_{FCLK}	Duty cycle		40	50	60	%
T_{start}	Start-up time	24MHz	191.66	234.53	339.00	μs

Note:

1. It is recommended to give reference values with crystal
2. Current consumption could vary with oscillating frequency, RCC_HXTCR.HXTDRV=110.
3. The data is based on the evaluation result, and is not tested in the production.

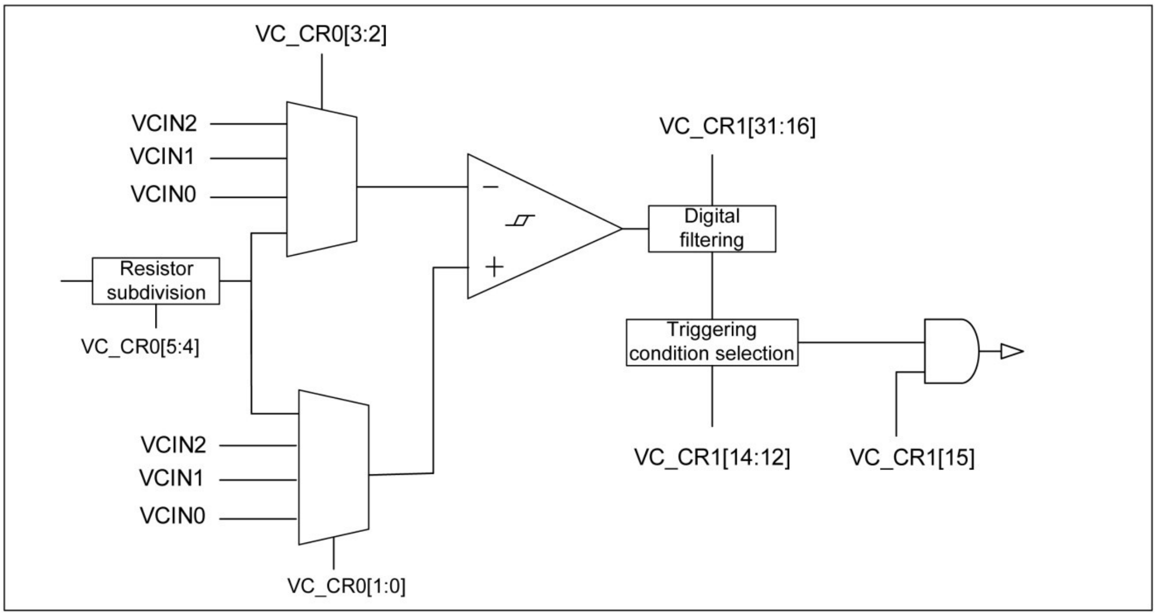
5.7 12-bit A/D converter



Symbol	**Parameter**	**Condition**	**Minimum value**	**Typical values**	**Maximum value**	**Unit**
V_{ADCIN}	Input voltage range	Single ended	0		VDD	V
V_{REF}	ADC reference Voltage			VDD		V
I_{ADC}			0.7	0.9	1.2	mA
C_{ADCIN}	ADC input capacitance		3.5	4	4.5	pF
F_{ADCCLK}	ADC clock Frequency		0.5	4	16	MHz
$T_{ADCSTART}$	Startup time of ADC bias current		2	3	4	μs
$T_{ADCCONV}$	Conversion time		16	16	20	cycles
ENOB			9.5	10	10.4	Bit
DNL	Differential non-linearity		-2	±1	2	LSB
INL	Integral non-linearity		-3	±1	3	LSB
E_o	Offset error		-2	±1	2	LSB
E_g	Gain error		-2	±1	2	LSB

Note: Designed by design, and not tested in the production.

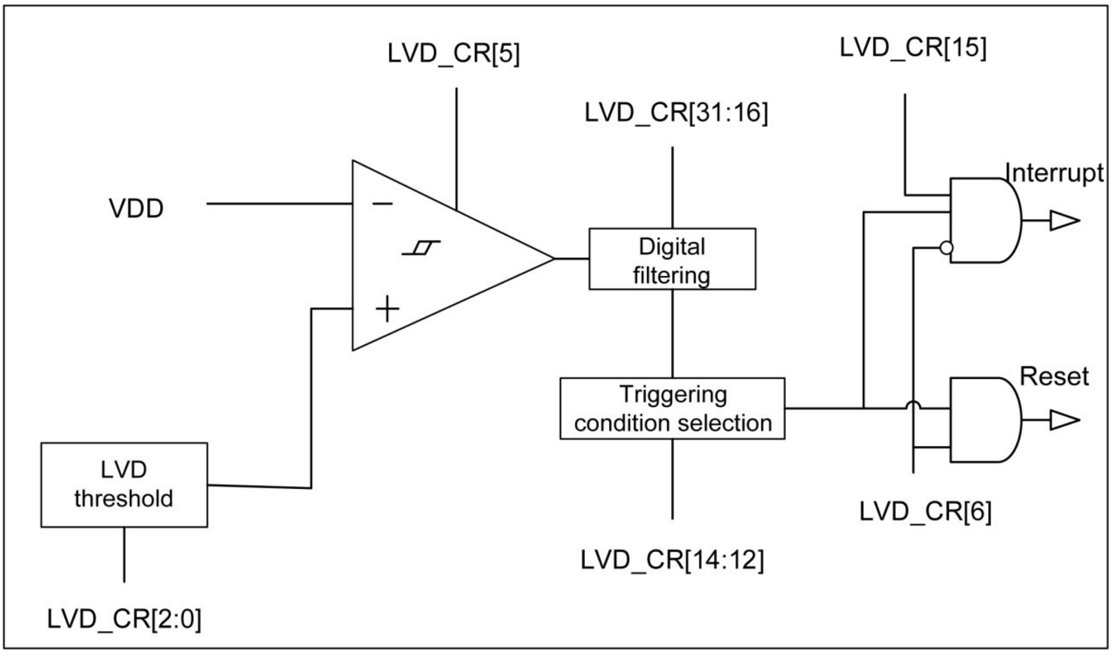
5.8 Analog voltage comparator



Symbol	Parameter	Condition	Minimum value	Typical values	Maximum value	Unit
V_{in}	Input voltage range		0		5.5	V
V_{incom}	Input common mode range		0		5.5	V
V_{offset}	Input offset		-10	±5	+10	mV
I_{comp}	Comparator's current			12		μA
$T_{response}$	Comparator's response			5		μs

Note: The data is based on the evaluation result, and is not tested in the production.

5.9 Low voltage detection features



Symbol	Parameter	Condition	Minimum value	Typical values	Maximum value	Unit
V_{level}	VDD Detectable threshold	LVD_CR[2:0] = 000 (4.4V)	4.20	4.39	4.54	V
		LVD_CR[2:0] = 001 (4.0V)	3.78	3.95	4.08	
		LVD_CR[2:0] = 010 (3.6V)	3.44	3.59	3.72	
		LVD_CR[2:0] = 011 (3.3V)	3.14	3.29	3.40	
		LVD_CR[2:0] = 100 (3.1V)	2.90	3.04	3.16	
		LVD_CR[2:0] = 101 (2.9V)	2.70	2.82	2.92	
		LVD_CR[2:0] = 110 (2.7V)	2.52	2.63	2.72	
		LVD_CR[2:0] = 111 (2.5V)	2.36	2.46	2.54	
I_{comp}	Detector's current		1	1.5	2	μA
$T_{response}$	Detector's response time when VDD fall below or rise above the threshold		30	50	80	μs
T_{setup}	Detector's setup time when ENABLE.VDD unchanged.		3	5	10	μs

Note: The data is based on the evaluation result, and is not tested in the production.

5.10 Memory erasing/writing features

Symbol	Parameter	Condition	Minimum value	Typical values	Maximum value	Unit
EC_{flash}	Sector Endurance		20k			cycles
RET_{flash}	Data Retention		20			Years
T_{prog}	Byte/Half Word/Word Program Time		30	45	60	μs
$T_{Sector\text{-}erase}$	Sector Erase Time		3.5	3.7	4.5	ms
$T_{Chip\text{-}erase}$	Chip Erase Time		20	30	40	ms

5.11 Wake-up time from low-power mode

The wake-up time means the wake-up time from Deep Sleep Mode by external interrupt. The time clock is HIRC. VDD=3.3V.

Symbol	Parameter	Condition	Minimum value	Typical values	Maximum value	Unit
T_{wakeup}	Deep sleep mode to active mode	HIRC Frequency: 4MHz 8MHz 16MHz 22.12MHz 24MHz		 11.5 7.5 5.2 4.5 4.2		μs

Note: The data is based on the evaluation result, and is not tested in the production.

5.12 Electromagnetic sensitivity

5.12.1 ESD

Symbol	Parameter	Condition	Minimum value	Typical values	Maximum value	Unit
$V_{ESD,\ HBM}$	ESD @ Human Body Mode		8			KV
$V_{ESD,\ CDM}$	ESD @ Charge Device Mode		1.5			KV
$V_{ESD,\ MM}$	ESD @ Machine Mode		400			V
$I_{Latchup}$	Latch up current		100			mA

5.12.2 Static latch-up

To evaluate latch-up performance, it is necessary to conduct 2 complementary static latch-up tests on 3 samples:

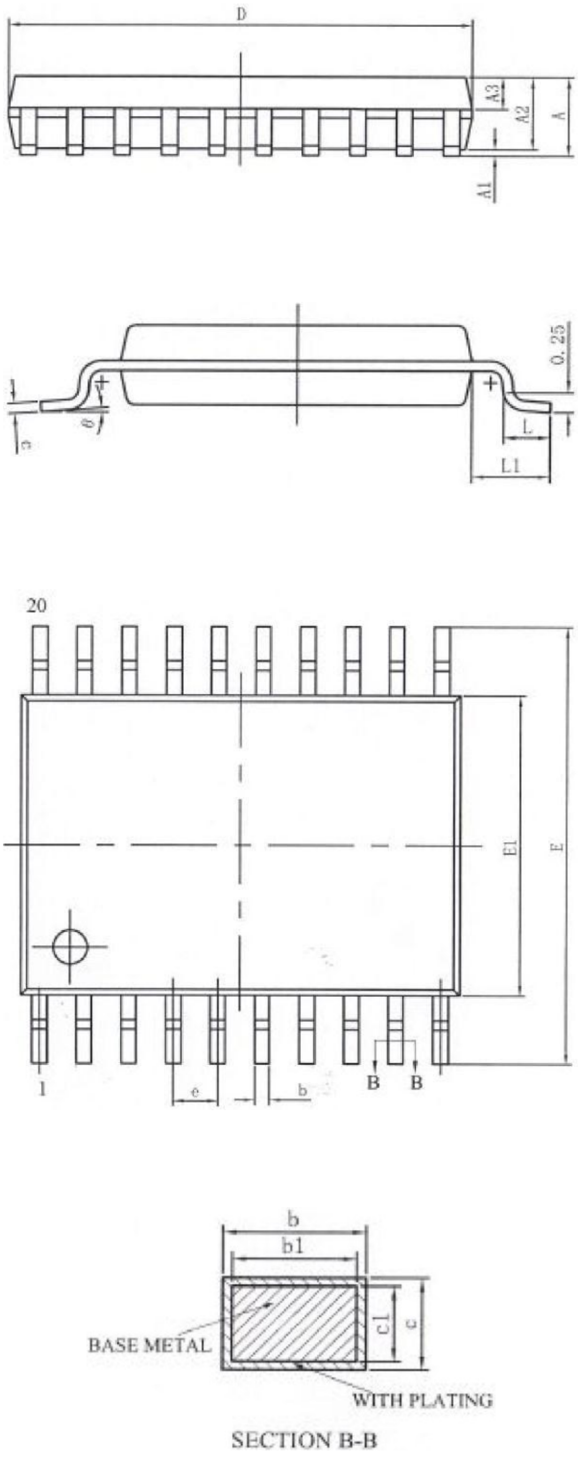
- Provide beyond-the-limit power voltage for each power supply pin.
- Inject current on each input, output and configurable I/O pin.

This test complies with EIA/JESD78A integrated circuit latch-up standards.

Symbol	Parameter	Condition	Type
LU	Static latch-up class	TA = +25 °C conforming to JESD78A	Class I Level A

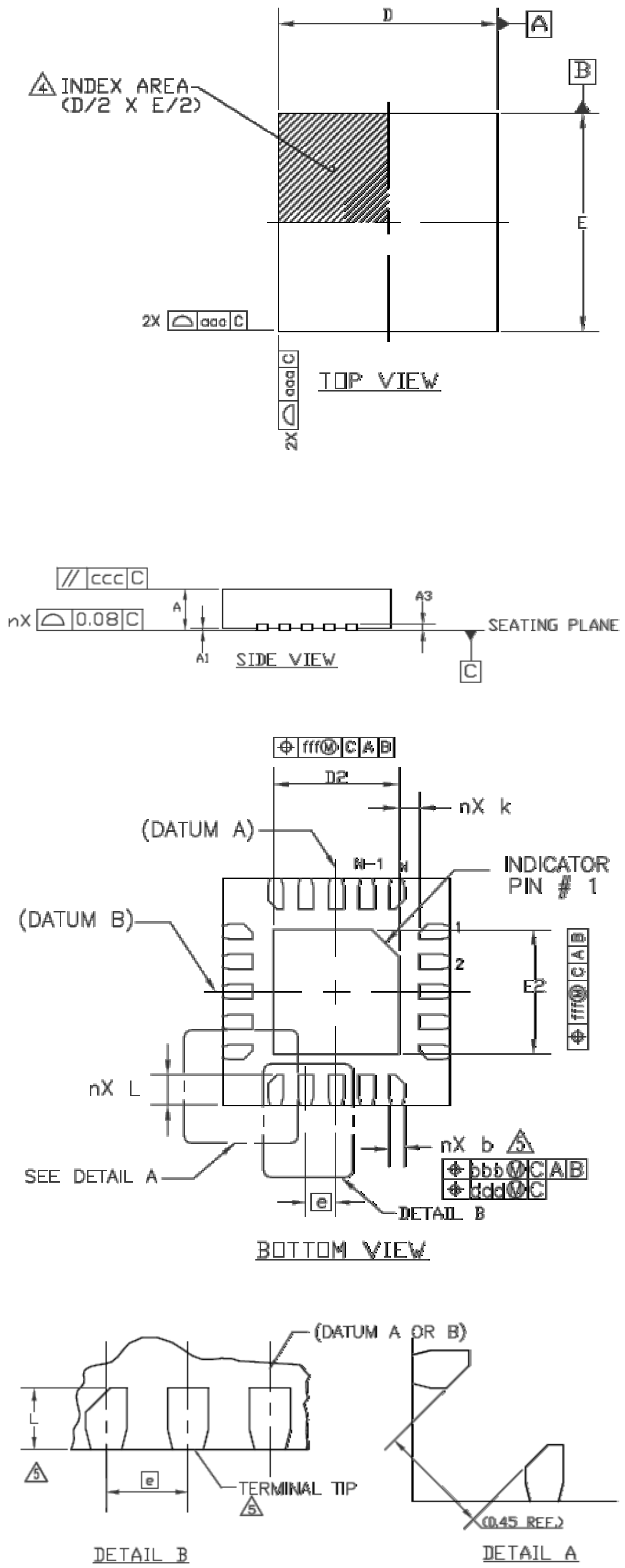
6 Package

6.1 TSSOP20



TSSOP20			
Symbol	Min	Nominal	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.29
b1	0.19	0.22	0.25
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC.		
L	0.45	0.60	0.75
L1	1.00 BSC.		
θ	0	-	8°

6.2 QFN20



QFN20			
Symbol	Min	Nominal	Max
A	0.70	0.75	0.80
b	0.15	0.20	0.25
D	3.00 BSC.		
D2	1.55	1.65	1.75
E	3.00 BSC.		
E2	1.55	1.65	1.75
e	0.40 BSC.		
L	0.30	0.40	0.50
n	20		
nD	5		
nE	5		
A1	0	0.02	0.05
A3	0.203 REF.		
K	0.20	-	-
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	

6.3 Silk screen

CX32L003F8
PP8825B
YYWWH

TSSOP20

- First line: The first 8 digits remain the same, the 9th digit represents the number of pins, and the 10th digit represents the Flash capacity. For details, refer to Part number scheming.
- Second line: The first 6 digits represent the Lot ID, and the 7th digit represent the product reversion.
- Third line: The first 4 digits represent the year and week for production, and the 5th digit represents the package test factory.

L003F8
PP8825B
YYWWH

QFN20

- First line: The first 4 digits remain the same, the 5th digit represents the number of pins, and the 6th digit represents the Flash capacity. For details, refer to Part number scheming.
- Second line: The first 6 digits represent the Lot ID, and the 7th digit represent the product reversion.
- Third line: The first 4 digits represent the year and week for production, and the 5th digit represents the package test factory.

7 Part number scheming

CX32 L 003 F 8 P 6 X

Device series

CX32 = 32-bit microcontroller

Product type

L = Low power model

Sub-series

003

Number of pins

F = 20pin
0 = KGD

Code capacity

6 = 32KB Flash
8 = 64KB Flash

Encapsulation

P = TSSOP
Q = QFN

Temperature

Temperature 6 = -40 °C to +85 °C

Packaging

U = Tube
R = Tray
T = Tape & Reel

8 Product selection table

Part Number	Flash (KB)	SRAM (KB)	Package	Packaging	A/T factory	Minimum packaging quantity (MPQ)	Minimum ordering quantity (MOQ)
CX32L003F8Q6R	64	4	QFN20	Tray	TSHT	490	29400
CX32L003F8P6U	64	4	TSSOP20	Tube	TSHT	5760	34560
					ANST	7000	56000
CX32L003F6Q6R	32	4	QFN20	Tray	TSHT	490	29400
CX32L003F6P6U	32	4	TSSOP20	Tube	TSHT	5760	34560
					ANST	7000	56000
CX32L003F8Q6T	64	4	QFN20	Tape & Reel	TSHT	3000	24000
					ANST	5000	40000
CX32L003F8P6T	64	4	TSSOP20	Tape & Reel	TSHT	4500 Note (1)	72000
					ANST	3000	24000
CX32L003F6Q6T	32	4	QFN20	Tape & Reel	TSHT	3000	24000
					ANST	5000	40000
CX32L003F6P6T	32	4	TSSOP20	Tape & Reel	TSHT	4500 Note (1)	72000
					ANST	3000	24000
CX32L00308	64	4	KGD	Note (2)	Note (2)	Note (2)	Note (2)
CX32L00306	32	4	KGD	Note (2)	Note (2)	Note (2)	Note (2)

Note:

1. The factory recommends 9,000 as MPQ if possible
2. Please contact the sales representative

9 Revision History

Version	Revision date	Summary of revisions
0.1	2019/5/10	Initial edition
0.2	2019/6/6	Update electrical characteristics
0.3	2019/6/13	Add ordering information
0.4	2019/7/3	Update model naming rule
0.5	2019/7/24	Update electrical characteristics Update ordering information
0.6	2019/9/5	Update electrical characteristics
0.7	2019/9/12	Document errata
0.8	2019/10/15	Errata ● Fig. 4-1 TSSOP20 pin configuration: X32K_IN and X32K_OUT errata Update ● Add 5.4Typical application block diagram ● 8 Product selection table: update information about packaging and test factory, MPQ and MOQ
1.0	2019/11/19	Update ● Update electrical characteristics ● Add 6.3 Official release 1.0